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Specification and Drawings, as originally filed, with Application for Patent Serial No: **2,301,973**, on March 21, 2000, by **SPACEBRIDGE NETWORKS CORPORATION,** assignee of Robert George Alexander Craig, Aneesh Dalvi and Marc Levesque, for "System and Method for Adaptive Slot-Mapping Input/Output Queuing for TDM/TDMA Systems".

Agent certificateur/Certifying Officer

June 26, 2001
Date

Canada

(CIPO 68)
01-12-00

OPIC CIPO

ABSTRACT

An input / output data queuing apparatus and method for data transfer between a control processor and a time division multiplex modem is disclosed. A plurality of queues within the modem is accessed through a queue selection block controlled by a timing control block that is in turn controlled via software. This allows directed multiplexing of specific data types into specific TDM transmission slots and retrieval and de-multiplexing of specific data types from the received TDM data stream. A plurality of processor queues feed each queue allowing prioritisation of the transmitted data elements. This eases processor requirements, maximises the use of the available transmission slots and provides an access mechanism that is adaptable to a wide range of system.

System and Method for Adaptive, Slot-Mapping Input/Output Queuing for TDM/TDMA Systems

FIELD OF THE INVENTION

The present invention relates to transferring data to and from a time division multiplex modems and is particularly concerned with easing the processor timing requirements within a control processor while ensuring correct mapping and retrieval of data into and from a slotted physical layer.

BACKGROUND OF THE INVENTION

An important element required for accessing a TDM(A) stream is the method whereby data is transferred in and out of the modem. Given a system implementation in which a specific functionality or data type is attributed to individual slots within the TDM scheme (for example, a broadband TDMA modem with traffic slots and signalling slots) this requires specific data from the control processor to be mapped into the appropriate TDM slots in the physical layer. For transmission, implementations in which both the data prioritisation and mapping to slots are carried out in the control processor are difficult. Either they establish a queuing order some time in advance of transmission or they require fine scale knowledge of the timing state of the modem in order to ensure that data is sent to the modem appropriately. If an advanced queuing order is established, lost transmit opportunities may result if data is received after the queuing order has been implemented. If fine scale knowledge of the timing state of the modulator is required, this increases the complexity of the processor interface and the software implementation in the control processor. Systems of the prior art are shown in US patent 4,355,388 by Deal issued October 19, 1982, US patent 5,926,458 by Yin issued July 20, 1999, and US patent 3,818,453 by Schmidt et. al., issued June 18, 1974.

A prior art implementation of multiple queue servicing is shown in Yin et. al.,. The prior art invention is concerned only with transmission of data packets from queues.

The Packet Scheduler of the prior art uses bandwidth and packet size

information to determine queue service times.

No TDM access scheme is implied by the prior art invention. The mechanism whereby elements from specific queues are placed in specific slots is therefore not indicated.

Given no data to transmit, the queues in the prior art invention are never serviced.

In a prior art implementation of a micro-programmable TDMA Terminal Controller, signalling and burst data are combined together to form a data burst which remains constant in size and format with time. Individual shift registers are used to multiplex or de-multiplex the data and signalling information in RAM into a single data element for transmission on / reception from a particular slot. No queuing capability is suggested by the prior art.

All bursts contain the same data type, therefore there is no need to map particular data types into particular slots; no programmability required for allowing different slot widths / formats.

It is therefore desirable to provide a queuing apparatus and process that overcomes the problems of the prior art.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide an improved process that ensures timely availability of correctly formatted data for multiplexing into individual transmit time slots, and allows de-multiplexing of the received time slots into separate data paths.

It is a further object of this invention to provide a programmable capability that allows the invention to be utilised within a variety of different systems.

An input / output data queuing apparatus and method for data transfer between a control processor and a time division multiplex modem is disclosed. A plurality of queues within the modem is accessed through a queue selection block controlled by a timing control block that is in turn controlled via software. This allows directed multiplexing of specific data types into specific TDM transmission slots and retrieval and de-multiplexing of specific data types from the received TDM data stream. A plurality of processor queues feed each queue allowing prioritisation of the transmitted data elements. This eases processor requirements, maximises the use of the available transmission slots and provides an access mechanism that is adaptable to a wide range of system.

The input queuing data transfer mechanism used in this implementation provides separate transmit queues in and the processor for different data types (or, equivalently, transmission slot types). By using a programmable queue selection engine and a high-resolution timing controller within the TDM modulator sub-system, correct mapping of the queued information into the specified slots is achieved. This includes the capability of combining data from several queues into a single data element for transmission on a specific slot. The multiple processor queues feeding a single queue allow data of the same type to be correctly prioritised before it is fed into the modulator.

On the receive path, a mechanism for separating the received data slots in such a manner that slots of the same functional group / data type can be handled in a similar manner should also be implemented. While this can be carried out using separate carriers and demodulators, providing this capability in a single demodulator reduces cost (since fewer modems are required) and can reduce bandwidth inefficiencies (since fewer

carriers are required). The output queuing data transfer mechanism used in this implementation provides separate modem receive queues for each data type. By using a programmable queue selection engine and a high-resolution timing controller within the TDM demodulator sub-system, the contents of specific data slots can be broken apart (if required) and placed in specific modem output queues. The data in the modem queues retrieved by the control processor through the processor interface, examined by the processor queue selection entity and passed onto one or more processor queues for access by a higher layer application.

In accordance with an aspect of the present invention there is provided:

A time division multiple access data transfer method for transmitting data in specified time slots in a TDM transmit stream and separating data from a received TDM stream, said method comprising:

A microprocessor within which software elements operate

A modem within which hardware elements operate

A plurality of processor queues into or from which said data flows,

A plurality of processor queue selection elements operatively connected to said processor queues

A plurality of modem queues with each said modem queue being operatively connected to one of said processor queue selection elements

A plurality of programmable modem idle queues

A programmable queue selection entity operatively connected to all said modem queues and idle queues

A programmable timing controller operatively connected to said programmable queue selection entity

A timing reference source operatively connected to said programmable timing controller

A burst time plan processor operatively connected to said programmable timing controller

Further features of the present invention will be apparent from the

ensuing description with reference to the accompanying diagrams to which, however, the scope of the invention is in no way limited.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1 illustrates, in a block diagram, the input queuing for transmit data in accordance with an embodiment of the present invention;

Figure 2 illustrates, in a block diagram, the output queuing for receive data in accordance with an embodiment of the present invention;

Figure 3 illustrates an example of a slotted access scheme with each slot numbered from 1 to N;

Figure 4 illustrates an exemplary system that uses the disclosed invention; and,

Figure 5 illustrates a prior art embodiment of a multiple queue servicing method.

DETAILED DESCRIPTION OF THE INVENTION

A multiple queue servicing system which is similar to the disclosed invention is shown in Figure 5. In this implementation, the Packet Scheduler assumes a similar functionality to the Timing Controller, and the Queue Server assumes a similar functionality to the combined Processor Queue Selection and Modem Queue Selection entities.

The time division multiple access data transfer apparatus for transmitting data in specified time slots in a time division multiplexed transmit stream and separating data from a received time division multiplexed stream according to the invention includes a microprocessor within which software elements operate, a modem within which hardware elements operate, a plurality of processor queues

implemented in software into or from which said data flows, a plurality of processor queue selection elements operatively connected to said processor queues, a plurality of modem queues with each said modem queue being operatively connected to one of said processor queue selection elements, a plurality of programmable modem idle queues, a programmable queue selection entity operatively connected to all said modem queues, a programmable timing controller operatively connected to said programmable queue selection entity and a burst time plan processor operatively connected to said programmable timing controller.

In an alternate embodiment of the present invention, the time division multiple access data transfer apparatus has a plurality of programmable modem idle queues operatively connected to the modem queue selection entity wherein the idle queues provide data to the queue selection entity when the associated modem queues are empty.

Referring to Figure 1, there is illustrated in a block diagram, input queuing in accordance with an embodiment of the present invention. A control microprocessor **9** communicates with the modem **10** through a processor interface **5**. A plurality of processor queues implemented in software **6** within the processor **9** use a processor queue selection entity **7** to transmit data over the processor interface **5** to a modem queue **1** in the modem **10**. A plurality of the modem queues **1** within the modem **5** are serialised into a single data stream **11** through a modem queue selection entity **2**. The Modem queue selection entity **2** is controlled via a timing controller **3** in the modem and via a burst time plan processor **8** in the processor. A timing reference **12** provides a time source for the timing controller. Each modem queue has an idle cell queue **4** associated with it that is also input to the Modem queue selection entity.

Data from a higher layer application is fed into the appropriate processor queue **6**. The processor queue selection entity waits for space to become available in the corresponding modem queue **1**. When space is available, the processor queue selection entity uses queue priority information to select a data element from one of the processor queues and passes it to the modem queue. The modem queue selection entity waits on a notification from the timer controller. This event signals which queues are to be

accessed to create a single data element which is to be inserted into the next upcoming transmission slot. The data element could be created by reading a programmed amount of data from a single queue or by reading a programmed amount of data from several queues in a serial fashion. Idle queues **4**, associated with each modem queue, with a programmed data element are accessed in the case that a particular modem queue is empty and data is to be read from it. The timing controller is programmed given knowledge of the format of the TDM stream slots. This information is maintained by the Burst Time Plan Processor **8**. Referring to Figure 3, a time division multiplex data stream consists of a collection of sequential slots (numbered 1 to N) containing data elements. The data elements carried within a slot may be of the same type or of a different type than the data within another slot. The slots themselves may be of the same or differing sizes. The correlation between data element type and slot is carried in a burst time plan table. The Burst Time Plan Processor contains this information and uses it to program the modem queue selection entity and the timing controller.

Referring to Figure 2, there is illustrated in a block diagram, output queuing in accordance with an embodiment of the present invention. A control microprocessor **9** communicates with the modem **10** through a processor interface **5**. A plurality of processor queues implemented in software **6** within the processor **9** receive data from a processor queue selection entity **7** over the processor interface **5** from a queue **1** in the modem **10**. A received data stream **11** is broken apart by a modem queue selection entity **2** and fed into a plurality of modem queues **1** within the modem **5**. The Modem queue selection entity **2** is controlled via a timing controller **3** in the modem and via a burst time plan processor **8** in the processor. A timing reference **12** provides a time source for the timing controller.

Data received on each time slot **11** is fed into the modem queue selection entity **2**. The modem queue selection entity is programmed to write data into one or more selected modem queues upon notification from the timing controller. As in the transmission case, the timing controller and the modem queue selection entity are programmed by the burst time plan processor using information contained within the burst time plan. The Modem queue selection entity notifies the corresponding processor queue selection entity that data is available. The processor queue selection entity retrieves

and examines the data and deposits it an appropriate processor queue. A higher layer application can then retrieve the data from the queue.

An example use of the invention is shown in figure 4. A broadband wireless network using a TDM forward channel and a TDMA return channel is depicted. This system consists of a base station control unit and multiple customer terminals. Within the base station there exists a control processor and a modem. Both input queuing and output queuing are used to provide the data path communication between the modem and the control processor. Similarly, within each terminal there exists a control processor and modem. Again both input queuing and output queuing are used to provide the data path communication required between the modem and the control processor.

Advantages of the present invention are as follows:

The disclosed invention addresses both transmission and reception of data.

A higher level hierarchical queuing exists, consisting of processor queues and modem queues in which prioritisation is carried out in the processor queues and slot mapping is carried out in the modem queues.

The modem queue selection entity (analogous to the Queue Server in the prior art) can be programmed to combine data from a number of modem queues into one data packet for transmission. The prior art Queue Server transmits data from a single queue at a time.

The disclosed invention's Timing Controller uses information contained within a burst time plan as passed to the invention from some master server system element.

Queues may be serviced and produce idle data in the case where no data is ready to be transmitted.

Software dictates data from queue (or *combination* of queues) that goes into which slot by control of the HW queue server via SW burst time plan processor, which is traditionally done under hardware control.

Variable length slot sizes supported.

Data from separate queues can be combined to fill a single slot, where traditionally single, fixed size queue fills a single slot.

Configurable idle data generation allowed on a per queue basis.

Ease of processor software requirements by separating data prioritisation (done in software) from slot mapping requirements (done in hardware under software control).

Allowance of directed multiplexing of particular data elements into specific transmission slots.

Allowance of data elements from more than one queue to be combined and transmitted as one data element.

Allowance of a single received data element to be decomposed into more than one data element, each data element then being placed in a separate receive queue.

Reduction of the size of modem queues required within the modem.

Adaptable to a variety of wireless TDM(A) system specifications.

The above-described embodiments of the invention are intended to be examples of the present invention. Alterations, modifications and variations may be effected the particular embodiments by those of skill in the art, without departing from the scope of the invention which is defined solely by the claims appended hereto.

We claim:

1. A system for queuing data in a digital modem comprising:

a processor queue selection entity for receiving data from a higher layer application;

a modem queue for receiving data from the processor queue selection entity; and

a timer controller for modifying a modem queue queue selection entity to access the modem queue.

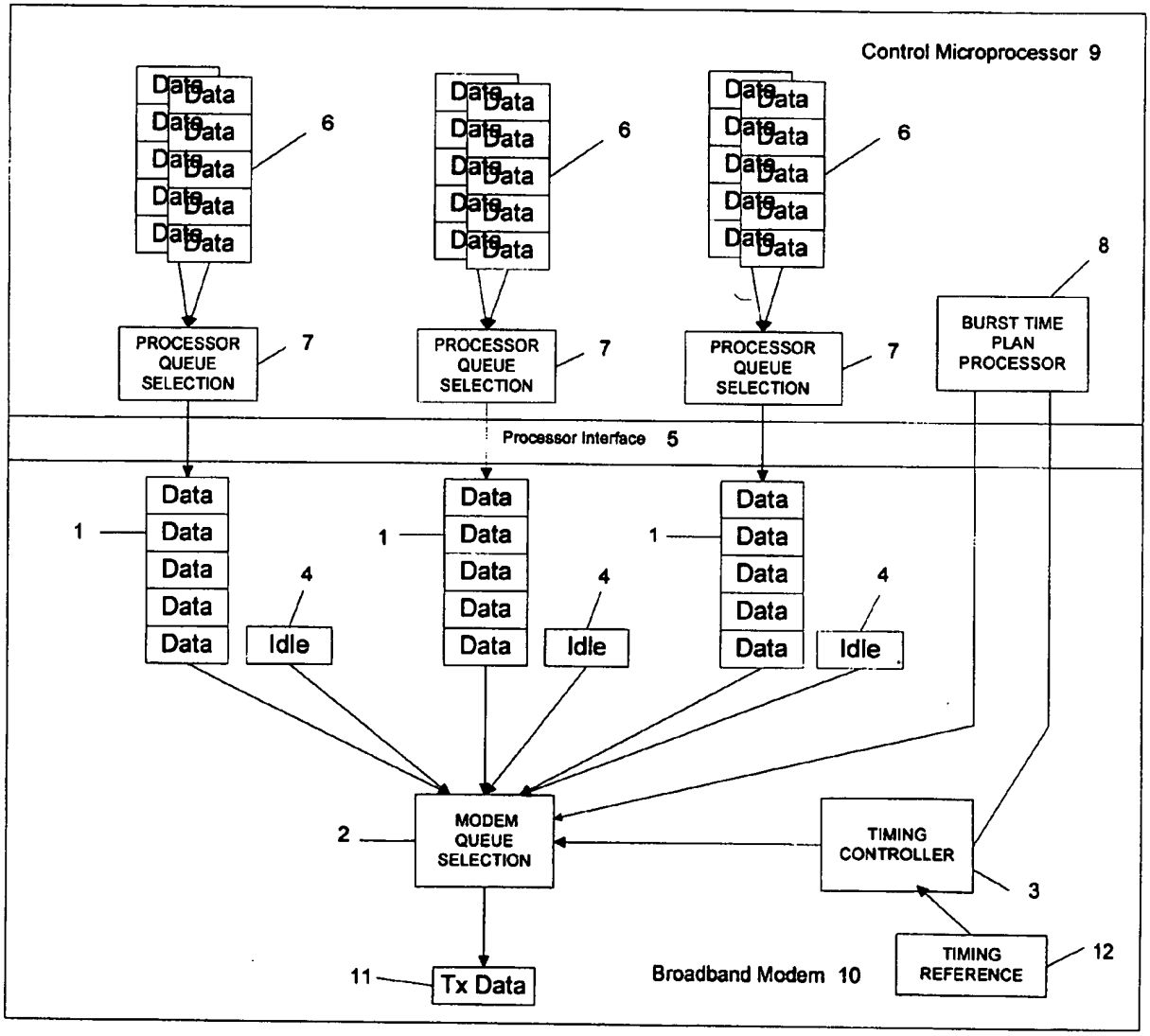
Control Microprocessor 9
Data
6
PROCESSOR QUEUE SELECTION
7
BURST TIME PLAN PROCESSOR
8
Processor Interface 5
1
4
Idle
MODEM QUEUE SELECTION
2
TIMING CONTROLLER
3
TIMING REFERENCE
12
11
Tx Data
Broadband Modem 10

Fig. 1

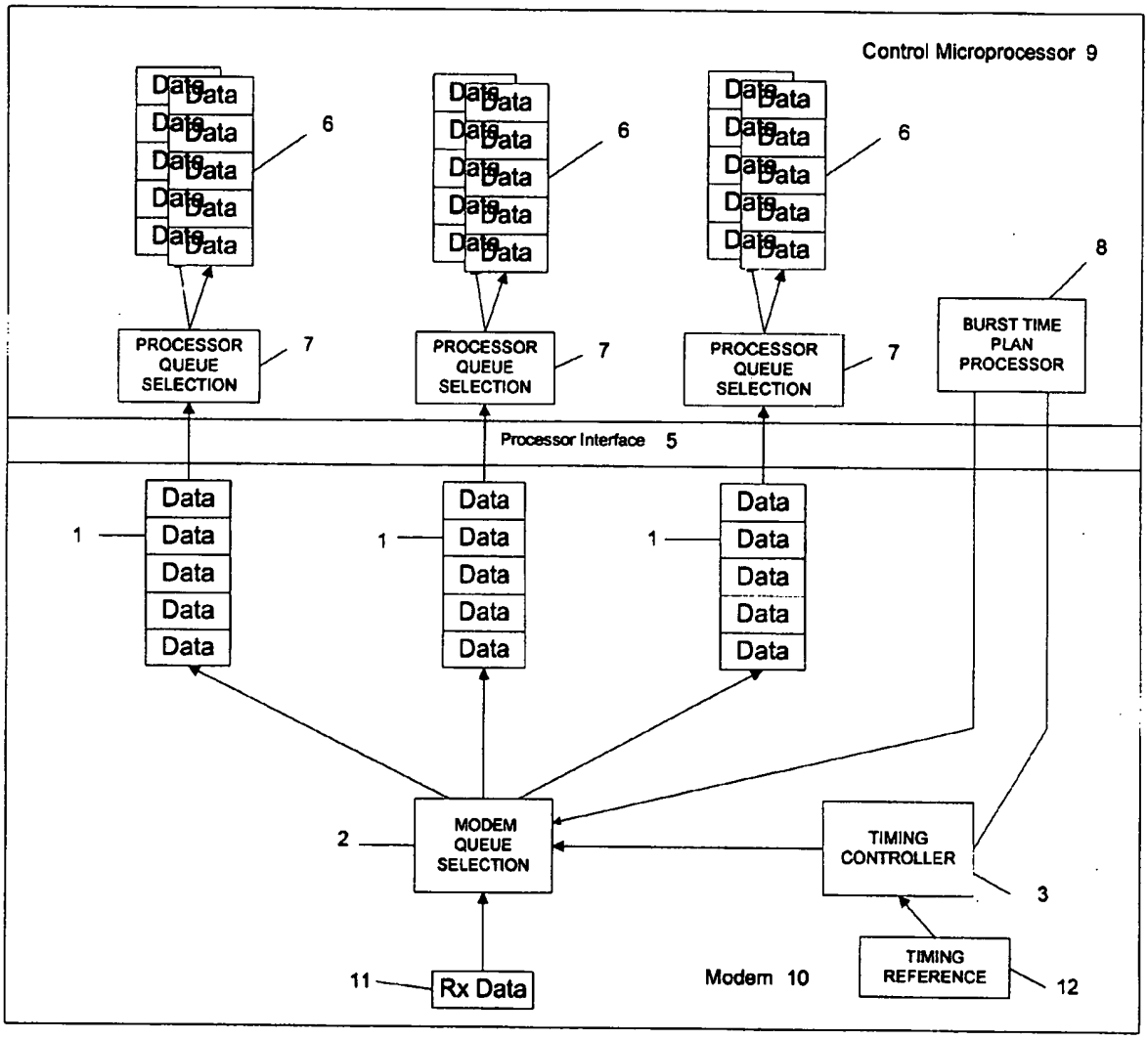
Control Microprocessor 9
Data
6
PROCESSOR QUEUE SELECTION
7
BURST TIME PLAN PROCESSOR
8
Processor Interface 5
1
MODEM QUEUE SELECTION
2
TIMING CONTROLLER
3
11
Rx Data
Modem 10
TIMING REFERENCE
12

Fig. 2

Fig. 3

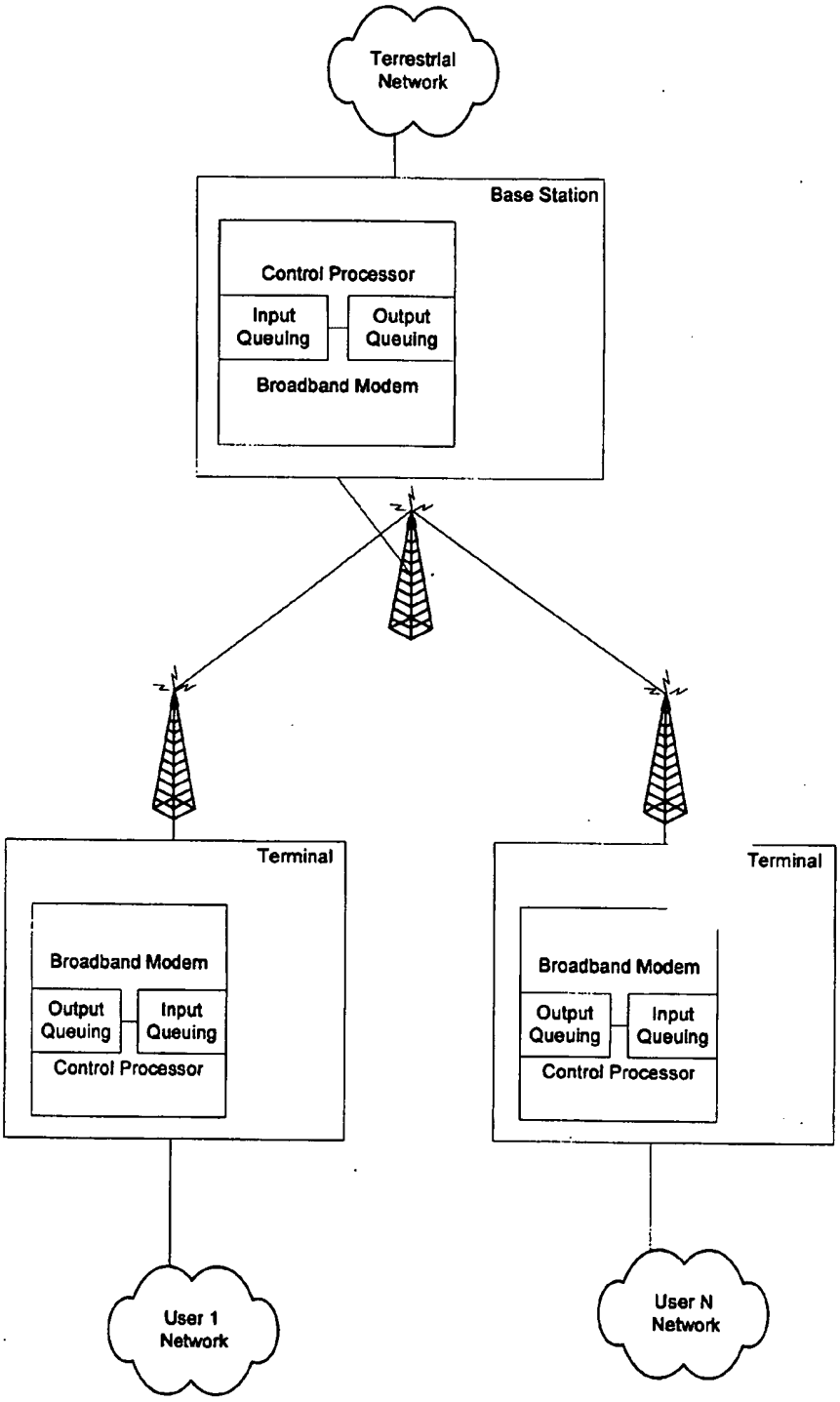
Terrestrial Network
Base Station
Control Processor
Input Queuing
Output Queuing
Broadband Modem
Terminal
Broadband Modem
Output Queuing
Input Queuing
Control Processor
Terminal
Broadband Modem
Output Queuing
Input Queuing
Control Processor
User 1 Network
User N Network

Fig. 4

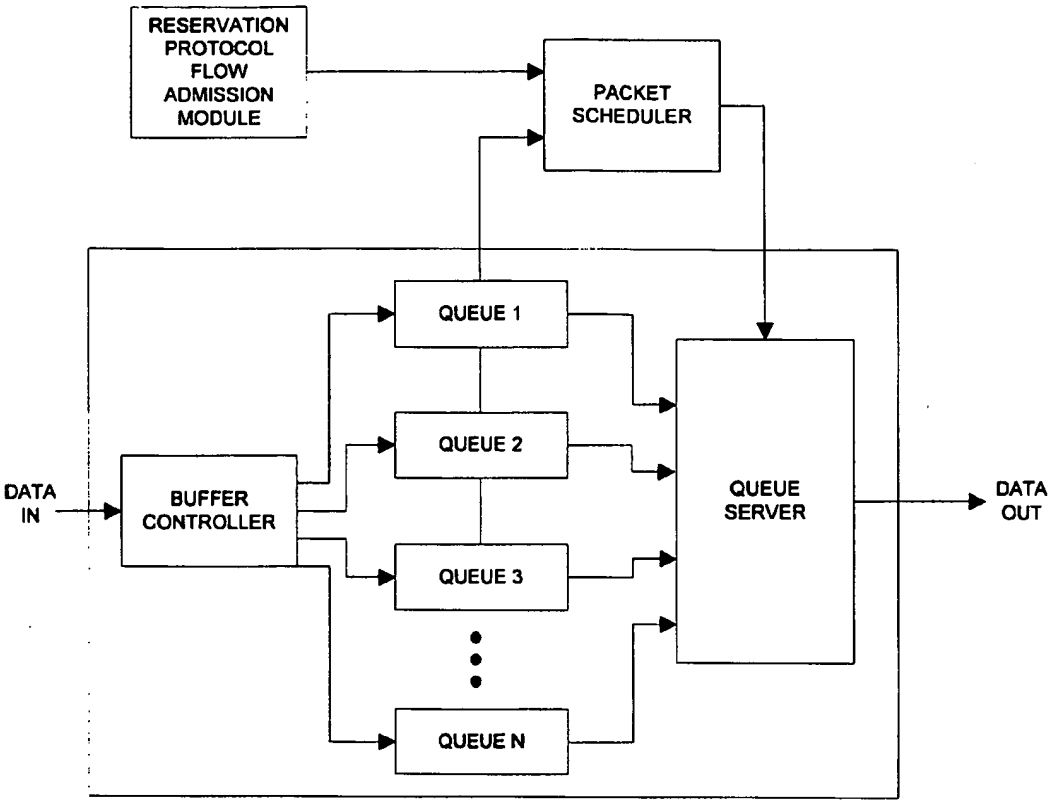

Fig. 5 (Prior Art)